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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,621	12/15/2003	Mitsuru Arai	OKI 399	8975
23995	7590	03/10/2006	EXAMINER	
RABIN & Berdo, PC 1101 14TH STREET, NW SUITE 500 WASHINGTON, DC 20005			NGUYEN, LONG T	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/734,621

Applicant(s)

ARAI ET AL.

Examiner

Long Nguyen

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 15 December 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 13-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 13-15, 17-20 and 22 is/are rejected.
- 7) ☒ Claim(s) 16 and 21 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 December 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 12/15/05.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Drawings***

1. The drawings are objected to because Figure 1-1 of the drawings fails to show the correct symbol for a PMOS transistor (for transistors T111-2, T111-2, T115-1 and T115-2). Note that the symbol of the transistors T111-2, T111-2, T115-1 and T115-2 as current provided in Figure 1-1 is for NMOS transistors, not PMOS transistors.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

Art Unit: 2816

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 13 is rejected under 35 U.S.C. 102(b) as being anticipated by Kohdaka (USP 5,329,172).

With respect to claim 1, Figure 1 of the Kohdaka reference discloses a chopper comparator, which includes: a first input terminal (A) for receiving an analog input signal (intended use, and input A is capable of receiving an analog signal), a second input terminal (B) for receiving a reference voltage (intended use, and input B is capable of receiving a reference voltage), a first switch (1); a second switch (1); a switch node (junction connection of switches 1 and 2 and capacitor 4); a comparator circuit output terminal (OUT); circuitry (4, 51-54, 3, 7) which includes a first stage (51-54, 3, 7) having a first input node (gates of transistors 53 and 51) and a first stage output node (drains of 53 and 51), the first stage comprising a gated inverter (51-54), and a first capacitor (4), wherein the gated inverter (51-54) includes: a first logic circuit transistor (PMOS 53), a second logic circuit transistor (NMOS 51), an intermediation connection node (drains of 53 and 51), a first current control transistor (PMOS 54) and a second current control transistor (NMOS 52), and an inverter (3) connected between the control electrodes of the first and second current control transistors (54 and 52).

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 13-15, 17-20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumamoto et al. (USP 5,936,434) in view of Kohdaka (USP 5,329,172).

Note that, each of Figures 2 and 28 of Kumamoto et al. discloses a comparator circuit, which includes: a first input terminal ( $V_{in}$ ) for receiving an analog input ( $V_{in}$ ); a second input terminal ( $V_{ref}$ ) for receiving a reference voltage ( $V_{ref}$ ); a first switch (S1); a second switch (S2); a switch node (junction of switch S1, S2 and capacitor C1); a comparator circuit output terminal ( $V_{out}$ ); circuitry connected between the switch node and the comparator circuit output (i.e., all the elements connected between the switch node and the comparator circuit output terminal  $V_{out}$ ), wherein the circuitry comprises a first stage (INV1 and INV11 in Figure 2; INV1 in Figure 28) having a first stage input node (node connected the inputs of INV1 and INV11 in Figure 2, node connected to input of INV1 in Figure 28) and a first stage output node (node connected the outputs of INV1 and INV11 in Figure 2, node connected to output of INV1 in Figure 28), and a first capacitor (C1); and the circuitry also includes a second stage (INV2 in Figure 2; INV2 and INV21 in Figure 28) having a second stage input node (node connected the input of INV2 in Figure 2, node connected to inputs of INV2 and INV21 in Figure 28) and a second stage output node (node connected to the output of INV2 in Figure 2, node connected to the outputs of INV2 and INV21 in Figure 28), and a second capacitor (C2); wherein the first stage (in Figure 2) includes a gated inverter (INV1, Figure 2) and another gated inverter (INV11, Figure 2), and the second stage (in Figure 28) includes an additional gated inverter (INV2, Figure 28) and a further gated inverter (INV21, Figure 28). Each of the Figures 2 and 28 of Kumamoto et al. does not disclose the detail of each of the gated inverter which each includes a first and second current control transistors. However, The Kohdaka reference discloses in Figure

Art Unit: 2816

1 a chopper comparator in which the clocked gated inverter (51-54, 3, 7) includes first and second current control transistors (54 and 52) and an inverter (3) connected between the first and second current control transistors (54 and 52) for the advantage of saving the power consumption (see Col. 3, lines 37-55, and Col. 5, lines 5-10). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the circuits in Figures 2 and 28 of the Kumamoto et al. reference by replacing each of the gated inverters in Figures 2 and 28 with a clocked gated inverter having first and second current control transistors (54 and 52) as taught by the Kohdaka reference for the purpose of saving the power consumption. Thus, each of the combination of Figures 2 and 28 of the Kumamoto et al. reference and the Kohdaka reference meets all the limitations of these claims (note that in the modification/combination of Figure 2 of Kumamoto et al., the first stage includes a gated inverter (INV1, Figure 2) and another gated inverter (INV11, Figure 2) wherein each of the gated inverter and the another gated inverter includes (from Figure 1 of Kohdaka) a first transistor (PMOS 53), a second transistor (NMOS 51), a first current control transistor (54), a second current control transistor (52), and an inverter (3); and in the modification/modification of Figure 28 of Kumamoto et al., the second stage includes an additional gated inverter (INV2, Figure 28) and a further gated inverter (INV21, Figure 28) wherein each of the additional gated inverter and the further gated inverter includes (from Figure 1 of Kohdaka) a first transistor (PMOS 53), a second transistor (NMOS 51), a first current control transistor (54), a second current control transistor (52), and an inverter (3)). Note that, each of Figures 2 and 28 also shows a switch (S3) connected between the first stage input node and the first stage output node (for claim 15) and a switch (S4) connected between the second stage input node and the second stage output node (For claim 20).

Art Unit: 2816

Also, for claim 22, the second stage output node (outputs of INV2 and INV21 in Figure 28) is connected to the comparator circuit output terminal Vout (by way of INV3 and INV31).

***Allowable Subject Matter***

6. Claims 16 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Response to Arguments***

7. Applicant's arguments filed on 12/12/05 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,


Art Unit: 2816

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



**LONG NGUYEN**  
**PRIMARY EXAMINER**